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Design of Multi-Level Inverter using CHB Connection

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ABSTRACT: In this world we have a huge demand for power with rapid development. As we have shortage of power we are implementing new techniques day by day to meet our daily demand. In our present paper we have come up with a new way of connecting separate dc sources in cascaded manner. In the present modeling 7-level H bridge cascaded is used. In our paper we are implementing symmetric inputs of dc voltage source to inverters. We are using three stages of dc sources to achieve seven levels of output as desired. The pulse width of the controlling signal can be designed as per the needs and switching frequencies. In this way we can further achieve high efficiency by reducing loses, number of switches and inverter size without any change in output of inverter.

KEYWORDS: PWM pulses, Multi-level inverter, H- Bridge, harmonic distortion, power quality

I. INTRODUCTION

Inverters are used to create the single phase or poly-phase AC voltages from the DC source of supply. The large inverters are used to drive adjustable speed motor Holtz, 1992 showed inverter with hard switching voltage source application producing PWM signals with sinusoidal fundamental. The common application "uninterruptable power supplies" (UPS) for computers and many loads. One of the most important performance considerations of power electronics circuits, like inverters, is their energy conversion efficiency.Inverters are widely used because they behave naturally as voltage sources as they are required by many industrial purposes. The inverter waveforms are required for some of the application such as static reactive power (VAR) compensation, active filters, and flexible ac transmission systems etc. According to the waveforms the topologies can be considered as voltage source inverters (VSI) where the voltage waveforms are independently controlled. Similarly the topologies can be current source inverters (CSI) where the output is current waveform. The modulating techniques ensure to control the time and sequence of the switch ON and switch OFF in the switching sequence. Some of the modulating techniques are sinusoidal pulsewidth modulation (SPWM), space vector technique (SV), selective harmonics eliminationtechnique (SHE). In inverter topologies, modulating techniques and control aspects, the DC link isconsidered to be purely DC or perfect DC. Nevertheless, some of the practical non idealconditions are also considered.

II. MULTI-LEVEL INVERTERS

The voltage source inverters produce an output voltage or a current with levels 0, +Vdcor-Vdc. They are known as two-level inverter.To obtain a quality voltage or a current waveform with a minimum amount of ripple content,they require high switching frequency along with various pulse width modulation (PWM)strategies.In high power and high voltage applications, these two level inverters, however, havesome limitations in operating at high frequency mainly due to switching losses and constraintsof device ratings.Moreover, the semiconductor switching devices should be used in such a manner as to avoidproblems associated with their series parallel combinations that are necessary to obtaincapability of handling high voltages and currents.Multilevel inverters have drawn tremendous interest in the power industry. They present a new set of features those are well suited to produce a near sinusoidal waveform. It may beEasier to produce a high power, high voltage inverter with multilevel structure because of theway in which device voltage stresses are controlled in the structure. Increasing the Number ofvoltage levels in the inverter without requiring higher ratings on individual Devices.The unique feature of multilevel inverters allows them to reach high voltages with lowharmonics without the use of transformers or series connected synchronous switching devices.As the number of voltage levels increases the harmonic content of the output voltage waveformdecreases significantly.

2.1 MULTI- LEVEL INVERTER CONCEPT

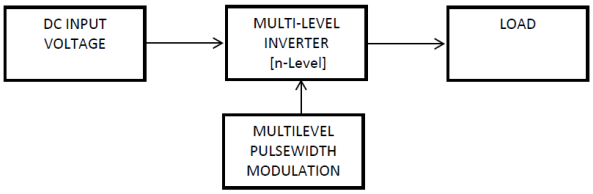

Fig 1

The output from the dc source is taken and fed to the n-level inverter which is controlled by the modulated pulses generated by any modulation technique or directly by any microcontroller. The output of the multi-level will be a near sine wave eliminating the lower order harmonics and hence addressing the power quality issues.

2.2 TYPES OF MULTI-LEVEL INVERTERS

2.2.1 DIODE CLAMPED MULTI-LEVEL INVERTER

This topology was first proposed in 1981. They are also known as neutral point inverters. In 1992 a lot of research work was published on Diode Clamped Multilevel Inverters. They have their fair share of advantages and disadvantages tied to them but then again, our firm faith in scientists and researchers has kept us calmly waiting for the better version of what we see today. As the name suggests, unlike Cascaded H-Bridge Inverters, they need clamping devices.Diodes are here used as clamping devices.Three phase diode clamped multilevel inverters have three legs with a common DC bus.This DC voltage is subdivided into switches via capacitors.For n-levels, n-1 switch pairs are required.One of the switches from each pair should be turned on.If one switch is turned on, the other one from the pair should be necessarily off.For n-levels, n-1 capacitors are required for clamping DC voltage.Switching devices (e.g. transistors) need to block only the supplied DC voltage; however the clamping diodes have a whole different story.Each diode has to block the voltage equal to number of switches above it times the supplied DC voltage.

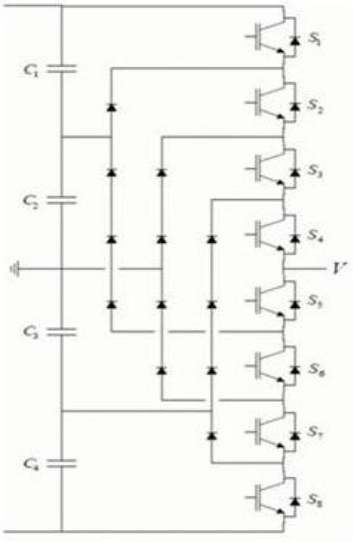

Fig 2

Advantages include high efficiency for switching at fundamental frequency, pre-charging of capacitors is done in groups. Especially, in three phase inverter; all three phases use a common DC bus which reduces the requirement of capacitance and supports efficient for back to back high power connections. It can also work with SDCs. Involves lesser cost and lesser number of components. Some of the demerits could be that quadratic relation between number of diodes and number of levels is difficult to calculate, especially when number of levels get higher it becomes stressful and you would surely want to avoid it.There is also difficulty in real power flow, maintaining certain charging and discharging is difficult.Charge balance gets disturbed for more than three levels which could in a way limit the output voltage.

2.2.2 FLYING CAPACITOR MULTI-LEVEL INVERTER

The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage

on each capacitor differs gives the size of the voltage steps in the output waveform. Fig 1.3 shows single phase n- level configuration of capacitor clamped inverter. An *n*-level inverter will require a total of (*n*-1)×(*n*-2)/2 clamping capacitors per phase leg in addition to (*n*-1) main dc bus capacitors**.** The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to $V_{dc}/(n-1)$, for an *n*-level inverter. The voltagesynthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clampedconverter.

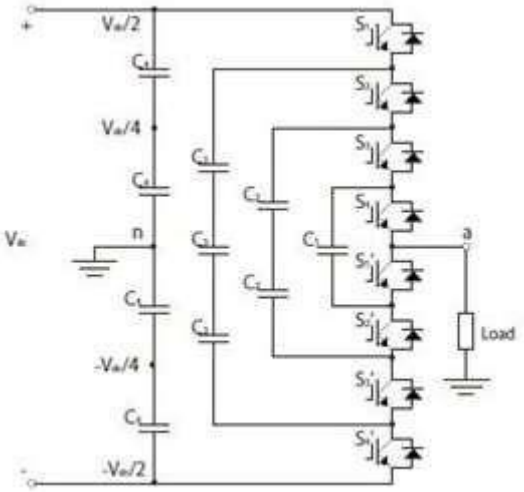

Fig 3 Flying Capacitor Multilevel Inverter

Advantages are that large amount of storage capacitors can provide capabilities during poweroutages.Both real and reactive power flow can becontrolled.Disadvantages are that excessive number of storage units is required when the number of levelincreases.They get bulky with the increase in number of stages and the inverter control can be verycomplicated.

2.2.3 CASCADED MULTI-LEVEL INVERTER

A cascaded multilevel inverter consists of a series of H-bridge (full bridge) inverterunits. The general function of this multilevel inverter is to synthesize a desired voltagefromseveral separate dc sources, which may be obtained from batteries, fuel cells or solar cells. Fig 4 shows the basic structure ofa single phase cascaded inverter with separate dc sources.Each separate dc source is connected to an H- bridge inverter. The ac terminal voltages ofdifferent inverters are connected in series.DC sources. The phase output voltage is synthesized by the sum of the inverter outputs, i.e., Vout I voutl + vout2 + vout3 +vout4. Each single-phase full bridgeinverter can generate three level outputs, +Vdc, O, and -Vdc. This is madepossible by connecting the DC sources sequentially to the AC side via the four gate-tum-offdevices.Each level of the full-bridge converter consists of four switches, Sl, S2, S3 and S4.Using the top level as the example, turning on Sl and S2, yields Vout=+Vdc. Turing onS3and S4 yields Vout=-Vdc. Turning off all switches yields Vout=0.Similarly, the acoutput voltage at each level can be obtained in the same manner. Minimum harmonicdistortion can be obtained by controlling the conducting angles at different inverter levels.For identical H-Bridges the modular structure is as follows, the number of levels in the line to load neutral of a star load will be p = 2k −1. The number of levels in the line-to-line voltage waveform will be k = 2N −1. The number of possible switch states is n states= N Phases.

The number of capacitors or isolated supplies required per phase isN cap = (N −1)/2.The number of switches in each leg is Sn= 2(N −1).Due to these advantages the CMI has wide applications such as High voltage DC transmission, Static VAR compensator, Stabilizer, High voltage and high power inversion because it has ability to stabilize the waveforms with better harmonic spectrum and low switching frequency.The number of output levels will be more than twice the number of DC sources. Layout issmall and packing is comfortable so manufacturing is quick and cheap. It has some disadvantages too. It uses separate DC sources for each H-Bridge so multiple separate DCsources are required.

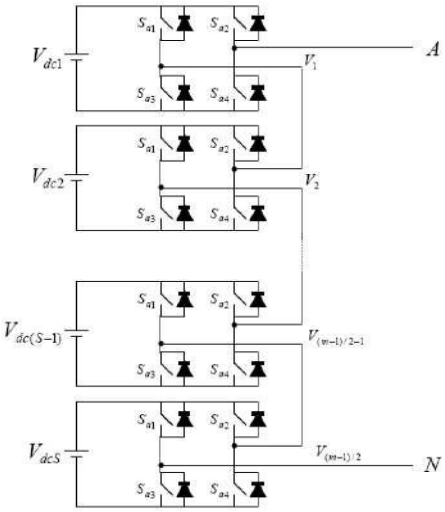

Fig 4. Equivalent circuit of cascaded multi-level inverter

III. WORKING, MODULATION TECHNIQUES &MODES OF OPERATION

A system of modulation in which the pulses are altered and controlled in order to represent the message to be communicated. There are different types of pulse modulation schemes. Among those the popular schemes are listed as follows: Pulse amplitude modulation (PAM): In PAM, the successive sample values of the analog signal are used to affect the amplitudes of a corresponding sequence ofpulses constant duration occurring at the sampling rate.Pulse width modulation (PWM): In PWM, the pulses representing successivesample values of analog signal have constant amplitudes but vary in time durationin direct proportion to the sample value.Pulse position modulation (PPM): In PPM, the sample values of analog signal areencoded by varying the position of a pulse of constant duration relative to itsnominal time of occurrence.Pulse width modulation is used widely as it involves the modulation of duty cycle to eitherconvey information over the communication channel or to control the amount ofpower sent to load. The advantages of PWM are listed as follows: the whole control circuit can be digital, eliminating the need for digital-to-analogconverters. Motors may be able to operate at lower speeds if controlling with PWM is done.When you use an analog current to control a motor, it will not produceconsiderable torque at low speeds.The output voltage control could be obtained without any additional components.With this technique, lower order harmonics can be eliminated or minimized along
with its output voltage control.

The generally used techniques are:Single pulse Width modulation, Multiple pulse Width modulation, Sinusoidal pulse width modulation, Modified Sinusoidal pulse width modulation andPhase displacement control.

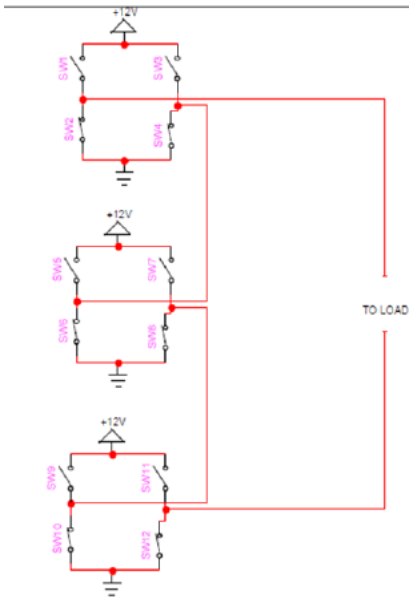

Fig. 7- level CHB inverter

The operation of this topology is quite similar as that of the single phase multilevelinverter topology. The bottom leg is similar that of 3 leg of the existing or standard invertertopology.Top of the hybrid H-Bridge inverter in series with the existing inverter leg. The H-Bridgecan use separate DC power source or can use a capacitor as the DC power source thenthe output of this topology is +Vdc or either –Vdcwith respect to ground. This leg is inconnection with a full H-bridge in series which in-turn is supplied by a voltage at capacitor. Ifthis capacitor is kept charged to Vdc.There is flexibility in choosing how output voltage is zero to regulate the capacitor voltage.Here only one DC power source is used in one inverter leg. So, the H-bridge uses a capacitor asthe dc power source.The switching pattern is as shown in the table 1 and accordingly the output waveforms dogenerate.

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V1	V2	V3	Vout
0	off	on	off	On	off	On	off	On	off	on	Off	on	0	0	0	0 V
Vdc	on	off	off	On	off	On	off	On	off	on	Off	on	12	0	0	12 V
2Vdc	on	off	off	On	on	Off	off	On	off	on	Off	on	12	12	0	24 V
3Vdc	on	off	off	On	on	Off	off	On	on	off	Off	on	12	12	12	36 V
-Vdc	off	on	off	On	off	On	off	On	off	on	On	off	0	0	-12	-12 V
-2Vdc	off	on	off	On	off	On	On	Off	off	on	On	off	0	-12	-12	-24 V
-3Vdc	off	on	On	off	off	On	On	Off	off	on	On	off	-12	-12	-12	-36 V

Table 1: Switching pattern for seven level inverter

IV. SIMULATION RESULTS

The design of the 7-level inverter using cascaded H-bridge connection was simulated, refer to fig 5. on the simulation software called 'Proteus'. The results obtained are as follows:

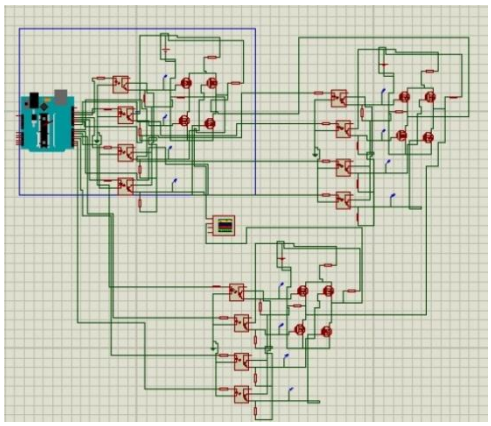

Fig 5. Simulation circuit

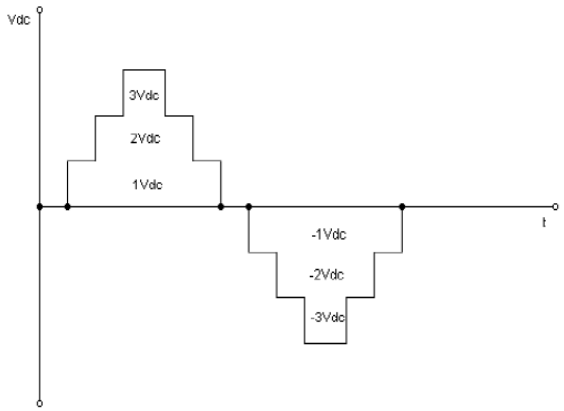

Fig 6. Output waveform

V. CONCLUSION

In this paper 7-level CHB inverter has been investigated to use only isolated DC sources.The multicarrier level-shiftedPWM technique has been adopted to integrate the voltagebalancing procedure using redundant switching states. The main advantage of this technique is its simplicity in hardwareimplementation using microcontrollers. The presented idea hasbeen simulated and results validated the good dynamicperformance of the voltage balancing process integrated into the switching technique. Different transient including changein DC source amplitude and load variations have been appliedon the running inverter and the capacitor voltage tracked thereference value acceptably. The main defect of this scheme isthe limited modulation index which will be investigated anddiscussed in future work. For testing symmetrical voltage stages can be tried and switching losses can be compared in order to state whether having multiple symmetrical sources is better compared to lesser asymmetrical sources to attaining different voltage levels at the output end.

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